REMARKS

Applicant respectfully traverses and requests reconsideration.

Applicant's attorney wishes to thank the Examiner for the courtesies extended during the telephone conference of March 18, 2008, and for reconsideration as discussed.

Applicant wishes to thank the Examiner for the notice that claim 20 would be allowable if rewritten in independent form. However as noted below, Applicant respectfully submits that the cited references each teach composite or partial frame rendering and do not teach alternate frame rendering as claimed and in fact, teach a less efficient and common approach and as such, Applicant respectfully submits that the claims are in condition for allowance.

For example, claim 30 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Walls in view of Lengyel. It is admitted that Walls teaches a composite frame generation approach wherein different displays and different processors are used to generate a portion of a large logical screen. It is alleged that "each graphics device is operable to render video for an entire screen for one display device" citing column 2, lines 39-41 and that each graphics device is considered to render an entire frame of video. However, as noted Walls actually teaches a composite display system that uses multiple remote computer systems to generate one entire scene or logical frame. Each remote computer generates a partial frame of an entire logical scene. Since the claim requires that, for example, "the first graphics device renders an entire frame of video, and wherein the second graphics device renders an entire second frame of video, and they are output over a common port, Walls cannot teach the claim subject matter since none of the computers generates an entire frame of video that are output over a common port. The claim cannot be parsed in an effort to render claim language obsolete. The claim must be interpreted in its entirety as written. The reference to an entire frame refers to an entire frame

that exits the common port. The Walls reference actually would require a plurality of independent ports, each outputting a different portion of a logical frame and as such, cannot teach the claimed subject matter. In fact, the Walls reference teaches a compositing technique wherein a processor merely generates a portion of a frame. Such systems are not as efficient or as fast typically as Applicant notes.

In the "Response to Arguments" section, the office action states that the Lengyel reference is merely used to teach first video output port coupled to a first video component output to a first graphics device and a first video component output to a second graphics device and that this teaching is incorporated into the Walls/Taylor combination. However the graphics device in Lengyel is actually a single graphics device whose pipeline is utilized to render portions of a frame. As such, both the Walls and the Lengyel reference teach composite processing of a single frame as opposed to an alternating frame rendering scheme as claimed. Lengyel does not disclose what is alleged. Applicant respectfully submits that the claim cannot be parsed in such a way as to change the meaning of the claim. The claims, require that the graphics device renders an entire frame of video and that the second graphics device renders an entire adjacent frame of video. The system of Lengyel uses a 3D pipeline to render a single frame by splitting the frame into scene layers. Accordingly, Applicant respectfully submits that the claims are in condition for allowance. Other differences will also be recognized by those of ordinary skill in the art.

Claim 29 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Walls in view of Lengyel, further in view of Taylor, further in view of Normile. Applicant respectfully reasserts the relevant remarks made above and as such, claim 29 is also in condition for allowance. Claim 29 requires alternate frame rendering by rendering an entire temporally

adjacent frame of video, provided the same output port. As noted above, the combination of references to not teach or suggest the claimed subject matter.

Claims 1 and 18 stand rejected under 103(a) as being unpatentable over Taylor in view of Normile. The "Response to Arguments" section states the following:

> In reply, the Examiner points out that bus 420 of Normile is considered to be the first video component output of the second video device (402), not frame buffer 430. Frame buffer 430 is considered to be the second video output port, not the first video component output of the second video device (402). Bus 420 is coupled to both a first video output port (425) (*shared memory 405 is coupled to bus 425 and is further coupled to bus 420*, Col. 9, lines 48-50) and a second video output port (430) (*frame buffer 430 is directly coupled to the video bus 420*, Col. 10, lines 7-11). The second video output port (430) is coupled to the first video component output (420) of the second video device (402) (*frame buffer 430 is directly coupled to the video bus 420, the structure of module 401 has equal application to each of the remaining compute modules such as 402-404, grant compute module 401 access to shared memory 405 over bus 420*, Col. 10, lines 7-11, 25-27, 55-57; *multiple video processing modules such as 401-404*, Col. 9, lines 11-15). Therefore, Normile teaches a first video device (401; *multiple video processing* modules *such as 401-404*, Col. 9, lines 11-15) having a first video component output (412) (*modules 401-404 are coupled to a computer system bus 425 via control bus 412*, Col. 9, lines 15-17); a second video device (402) having a first video component output (420) (*the structure of module 401 has equal application to each of the remaining compute modules such as 402-404, grant compute module 401 access to shared memory 405 over bus 420*, Col. 10, lines 25-27, 55-57); a first video output port (425) coupled to the first video component output (412) of the first video device (401) (*modules 401-404 are coupled to a computer system bus 425 via control bus 412*, Col. 9, lines 15-17) and the first video component output (420) of the second video device (402) (*shared memory 405 is coupled to bus 425 and is further coupled to bus 420*, Col. 9, lines 48-50; Col. 10, lines 25-27, 55-57); and a second video output port (430) coupled to the first video component output (420) of the second video device (402) (*frame buffer 430 is directly coupled to the video bus 420*, Col. 10, lines 7-11, 25-27, 55-57), as recited in Claim 1.

However, Applicant respectfully submits that the claim interpretation appears to be inconsistent with both the Applicant's Specification and with the references themselves. By way of example, the Specification refers to video output ports as a connection point with, for example, displays or interfaces for displays and are shown by way of example as connectors that

may be, for example, employed on a printed circuit board, on a device etc. as known in the art or are nodes configured as a connection node to which a display is coupled that receives the video component output and display synchronization information. The office action alleges that the frame buffer 430 is a "second video output port". However, as known in the art, a frame buffer is not a video output port – it is a frame buffer. This is supported by the Normile reference itself since it only refers to the frame buffer 430 as a frame buffer. There is no reference in Normile to the frame buffer 430 as being any video output port. In addition, Applicant's own Specification also refers to frame buffer (see for example, page 8, line 25) which is shown by way of example as part of the video RAM 122 which also is shown not to be the video output ports 152 and 151, for example. As such, since the interpretation is inconsistent with both Applicant's Specification and the cited reference, Applicant respectfully submits that the claims are in condition for allowance.

In addition, if the claims are not passed to allowance, Applicant respectfully requests a source of the definition used by the Patent Office to reject Applicant's claim and respectfully requests support for the definition used of the "first video output port" and "second video output port" as the cited reference does not teach this subject matter. Also Applicant respectfully notes that it is improper to interpret a claim to be inconsistent with Applicant's Specification.

Other interpretations appear to be improper. For example, the claim refers to "a first video output component signal". However, the office action does not address this claim language but instead attempts to render the claim unpatentable by misinterpreting the claims in the cited reference. For example, as stated above, it is alleged that the bus 420 of Normile is "considered to be the first video component output". However, the claim requires that the first video component output "provide a first video output component signal". This does not appear

to be addressed in the office action. In any event, the office action on the one hand alleges that a video output port is a "frame buffer 430" and then on the other hand, alleges that a video output port is a "bus". It is respectfully submitted that the claim interpretation must be consistent.

The claim requires that the first video output port is coupled to the first video component output of the graphics device and the first video component output of the second graphics device. Since bus 420 is alleged to be the first video component output of the second video device, the claim would require that bus 420 is coupled to bus 425. The office action alleges that these two buses are coupled. However, as specifically shown in Normile and as stated in Normile, bus 425 does not provide data to bus 420 nor does bus 420 provide data on the bus 425. To the contrary, bus 420 provides information to the frame buffer 430 and the shared memory 405 as shown, for example, in the cited FIG. 4. In fact, it is bus 412 of Normile that is coupled to bus 425. Alleging that bus 420 is coupled to bus 425 is inconsistent wit the Normile design. As such, Applicant respectfully submits that the Normile reference appears to have been misapprehended as well as Applicant's claim language. Accordingly, the claims are in condition for allowance.

As to claim 18 the claim requires that a monitor is coupled to the first video output port again confirming Applicant's previous remarks above that the video output port is a connection point for a monitor. The interpretation of Normile with respect to claim 1 is inconsistent with the interpretation being taken with respect to claim 18 which cites to Taylor since the alleged video output ports for which Normile is cited as teaching, would require a monitor to be coupled to bus 425 which clearly it is not as shown in Normile. In fact, Normile is coupled to frame buffers 427 or 430. Accordingly, this claim is also in condition for allowance.

Applicant also respectfully reasserts the relevant remarks made in the previous response.

Claims 19, 21 and 22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Taylor in view of Deering. Applicant has amended the claim to include inherent language illustrating that the first and second signals which are representative of first video output components are signals that represent color component information (see for example, page 11, lines 1-11 and elsewhere). As such, the adjustment of the second device until the value of the second signal at the first output node matches the determined value of the first signal at the first output mode is with respect to the color component values of the video signal – not timing or synchronization signals. Accordingly the claims are in condition for allowance.

Applicant also respectfully reasserts the relevant remarks from the previous response and also notes that the Deering reference has been cited as teaching the adjusting operation. However, the claim requires adjusting the value of the second signal which represents color component information, to match the determined value of the first signal which also represents color component information, at the first output node. The cited portion of Deering, among other differences, actually refers to attempting to match video synchronization signals between multiple displays. This is distinctly different from attempting to match the color component values corresponding to pixel information that is displayed. Accordingly, Applicant respectfully submits that Deering does not teach the claimed subject matter that Taylor is missing and as such, these claims are also in condition for allowance.

Claims 31, 38 and 39 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Walls and Lengyel in view of Taylor. Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

Claim 32 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Walls, Lengyel, Taylor and Deering. Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

Claims 33, 34, 36 and 37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Walls and Lengyel in view of Deering. Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

Claim 35 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Walls and Lengyel in view of Eichenberger. Applicant respectfully reasserts the relevant remarks made above and as such, this claim is also in condition for allowance.

Applicant respectfully submits that the claims are in condition for allowance and respectfully requests that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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